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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,330	07/14/2003	Frederik Eaton	FULCP004X1	7945

22434 7590 03/04/2004	EXAMINER
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ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)
Office Action Summary		10/620,330	EATON ET AL.
		Examiner	**Art Unit**	
		Helen B Rossoshek	2825	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2003*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-12,14,15,17-23,27-31,33 and 34* is/are rejected.

7)☒ Claim(s) *13,16,24-26 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All   b)☐ Some * c)☐ None of:

　　　1.☐ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
　　　application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
　　Paper No(s)/Mail Date *09242003*.

4) ☐ Interview Summary (PTO-413)
　　Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

Non-initialed and/or non-dated alterations have been made to the oath or declaration. See 37 CFR 1.52(c).

Claim Objections

2. Claims 1, 14, 33 are objected to because of the following informalities:

The limitation "sizing transistors ... at least one transistor dimension" of the claim1 and claim 14 are formulated unclear to what applicant intent to mean.

Claim 33 line 2 after "which" insert –when executed by a computer--

Appropriate correction is required.

3. Claims 30, 31, 32 and 34 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 1, which claims 30, 31, 32 and 34 depend from, fails to show any design steps of generation of netlist and/or a step of a circuit design (claims 30, 34) (instead a preamble of claim 1 reads as a method for facilitating **physical synthesis of a circuit design**).

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claim 31 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Data structures are descriptive material and are not statutory if not claimed as embodied (executed) in computer-readable media, because without executing the data structures are not capable of causing functional change in the computer.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 31 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-6, 9, 11, 14, 15, 17-23, 27, 28, 30, 33 and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Karniewicz (US Patent Application Publication 2002/0023255).

With respect to claim 1 Karniewicz teaches sizing transistors in each of the cell instances with reference to an objective function thereby resulting in a first plurality of cell subtypes for each cell type, each cell subtype corresponding to a particular cell type differing from all other cell subtypes corresponding to the particular cell type by at least one transistor dimension as shown on the Fig. 1(a) wherein the basic hierarchical structure depicted including cell instances (102, 104, 106) resulting in a first plurality of cell subtypes (1, 2, 3) corresponding to a particular cell type having a difference in cell subtypes by at least one parameter and as a result of such structure, transistors of different sizes and shapes can be created (paragraph [0028], paragraph [0029], paragraph [0031], paragraph [0008]); and merging selected ones of the subtypes for at least one of the cell types thereby resulting in a second plurality of subtypes for the at least one of the cell types, the second plurality of subtypes being fewer than the first plurality of subtypes, wherein merging of the selected subtypes achieves a balance between the objective function and a cost associated with maintaining the selected subtypes distinct as shown on the Fig. 1(b) wherein subtypes cells (134, 136,138, subtypes 1 and 3) and cell of type 1 (132) have a set of parameters related to its type and grouped in one cell (device) (132) comparing to the cell 100 on the Fig. 1(a) (paragraph [0031], paragraph [0032], paragraph [0078]).

With respect to claims 2-6, 9, 11, 14, 15, 17-23, 27, 28, 30, 33 and 34 Gheewala et al. teaches partitioning the cell instances for each cell type into at least one instance class, the cell instances In each instance class having a same relationship to an immediate parent cell, each instance class corresponding to one of the first plurality of subtypes as shown on the Fig. 1(b) wherein each of cell (132) (parent cell of type 1) and cells (134, 136, 138) (instances of cell type 1 and 3) have a set of parameters related to its type (paragraph [0031]) in the first plurality of subtypes of the type 1 (132); the partitioning of the cell instances is performed with reference to at least one user-defined constraint (paragraph [0054]); the partitioning of cell instances is performed prior to the sizing of the transistors; the partitioning of cell instances is performed after the sizing of the transistors within an software design framework II (DF2) for allowing a designer of semiconductors to create customized instances of pcell (type cell) and providing a control of transistors parameters (splitting or grouping or changing width, length, i.e. size) (paragraph [0004]); the merging of the selected subtypes is performed with reference to the instance classes as shown on the Fig. 1(b) cells (134) and (138) are instances of cells of type 1 as have been defined as cell (100) of Fig. 1(a) (paragraph [0039]); the merging of the selected subtypes is performed with reference to a distance function which represents a distance between two of the selected subtypes in a metric space which relates the objective function and the cost within software which allows manipulate with cells and creating parameterized instances for implementing the geometry demonstrated on the Fig. 5 (paragraph [0004], paragraph [0054]); a decision to merge the selected subtypes is made by comparing

the distance between the two selected subtypes to a threshold value within the software (DF2) for designing the semiconductors structures allowing the control of the size, parameters, orientation, shifting of the connections including meeting the specific design rule requirements (paragraph [0054], paragraph [0082]); at least one of the selected subtypes corresponds to a fixed-size subtype, the threshold value to which the distance between the fixed-size subtype and others of the selected subtypes is compared being different than the threshold value employed for comparisons among the other selected subtypes within the pcell (paragraph0054]) as shown on the Fig. 5 and shift parameters for determination of the relative orientation of the cell subtype 3 and cell subtype 2, wherein the alignment can be controlled (paragraph [0076], paragraph [0077]); the objective function comprises at least one area and power dissipation (paragraph [0003]); the merging of the selected subtypes is performed with reference to at least one internal characteristic of the selected subtypes within parametrizing the pcell wherein the parameters can be specified (paragraph 0054]); the at least one internal characteristic comprises transistor sizes (paragraph [0004]); the merging of the selected subtypes is performed with reference to at least one external characteristic of the selected subtypes within consideration of the relationship between two cells , which were manipulated by the software DF2 (paragraph [0076]); the at least one external characteristic comprises at least one of external resistive loads for the selected subtypes, and external capacitive loads for the selected subtypes (paragraph [0074]); further comprising, prior to sizing the transistors, partitioning the cell instances for each cell type into the first plurality of subtypes as shown on the Fig. 1(a) wherein the cell

(100) is presented as smaller cells (atoms) (102, 104,106, 108), which constituent the higher-order cell (paragraph [0029]); the partitioning of the cell instances comprises making subtype assignments for parent cell instances on a first level of a hierarchy of the circuit design with reference to a number of parent cell subtypes, and estimated subtype counts for child cell instances in the parent cell instances on at least one other level of the hierarchy below the first level the basic hierarchical structure shown on the Fig. 1(a0, 1(b), 1(c), wherein parent cell (100) defined as a set of child cells (102, 104, 106, 108) on the different level of the hierarchy and different subtypes (paragraph [0032]; Page 9, claim 17); each of the subtype assignments for the parent cell instances is made with reference to a profit function representing a profit corresponding to the subtype assignment (Page 9, claim 20); further comprising mapping the first plurality of subtypes into a metric space which relates the objective function and the cost as shown on the Fig. 5 and 6 wherein the geometry (502) was determined by having the associated parameters in the metric space (such as lx , ly) (paragraph [0056], paragraph [0071]); comprising weighting each of the first plurality of subtypes in accordance with a number of the cell instances corresponding thereto by having a plurality of sets of parameters (weighting) corresponding to an instance (cell instance) of an abstraction (first plurality of subtypes) (paragraph [0007]); an integrated circuit desired according to the method of claim 1 (paragraph [0003]); at least one computer-readable medium having computer program instructions stored therein which are operable to perform the method of claim 1 (paragraph [0010]); an electronic system

comprising at least one integrated circuit designed according to the method of claim 1

(paragraph [0010]).

Claim Rejections - 35 USC § 103

10.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11.   Claims 7,8, 10, 12, 16, 24 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Karniewicz as applied to claims 1, 9 and 21-23 above, and further in

view of Gheewala et al. (US Patent 6,445,065).

Wit respect to claims 7, 8, 10, 12, 16 and 24 Karniewicz teaches the limitations

from which the claims depend. However Karniewicz lacks the specifics regarding

asynchronous circuit, layout cost. Gheewala et al. teaches the circuit design

corresponds to an asynchronous circuit; the circuit design corresponds to a

synchronous circuit within providing a user customizable integrated circuit with

synchronous and asynchronous functional units and layout architectures for clocking

traces (col. 3, II.4-8); the distance function comprises a plurality of components which

includes any of a layout cost corresponding to the selected subtypes, a number of

instances of each of the selected subtypes, transistor sizes for the selected subtypes,

estimated transistor sizes for a merged subtype, external resistive loads for the selected

subtypes, and external capacitive loads for the selected subtypes (col. 7, II.49-55) by

using the new gate feature density (distance function) such as specific regions of an

integrated circuit (synchronous and asynchronous) with defining a set of different type of cells and manipulating with them and relating to a lower mask cost (col. 2, II.64-67; col. 3, II.1-3); the threshold value represents a tradeoff between the objective function and the cost as shown on the Fig. 13 using programmable core cells (basic cells) allows saving the cost (very little metal), power dissipation (real estate), but increases the length (density) of connection between cells (devices) (distance) (col. 13, II.65-67; col. 14, II.1-4). It would have been obvious to one of ordinary skill on the art at the time the invention was made to have used Gheewala et al. to teach the specifics subject matter Karniewicz does not teach, because a user customizable integrated circuit architecture having regions for different types of core cells including placement an routing of the individual cells may be more efficiently completed (col. 3, II.21-22).

12.   Claims 29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karniewicz as applied to claim 1 above, and further in view of Pullela et al. (US Patent 5,790,415).

With respect to claims 29 and 31 Karniewicz teaches the limitations from which the claims depend. However Karniewicz lacks the specifics regarding generating a netlist as claimed. Pullela et al. teaches generating a set of path between observable nodes in a netlist representing the circuit design, each path corresponding to a sequence of signal transitions by analyzing a plurality of paths (set of paths) and each node of the integrated circuit (netlist) for identifying the "critical path" in accordance with the user constraint (required time delay) for the optimization of the netlist (col. 2, II.47-51, II.55-67; col. 4, II.10-15); and sizing transistors represented in the netlist to attempt

to meet a delay constraint for each path, the delay constraint corresponding to a unit delay times the number of signal transistors in the corresponding path, a plurality of individual delays of different durations being allocated among the transitions for at least one of the paths to meet the delay constraint, at least one of the individual delays exceeding the unit delay by creating a transistor model (col. 9, ll.60-64; col. 14, ll.41-42; col. 3, ll.54-59), wherein the sizing of each transistor is done for each signal transition in the model in order to meet a delay constraint (requirement) by calculating slack (the difference between arrival time and required time) for each input/output in the circuit (in the path) as shown on the Fig. 2 (col. 3, ll.54-59); at least one computer readable medium having data structures stored therein representing a sized netlist generated according to the method of claim 1 within the computer aided design program which allows to store the netlist as a design file (col. 5, ll.24-27). It would have been obvious to one of ordinary skill on the art at the time the invention was made to have used Pullela et al. to teach the specifics subject matter Karniewicz does not teach, because speed and silicon area for integrated circuits being designed, there is also a continuing need to optimize the design process itself which provides the optimized netlist, such that the desired circuit netlist and circuit optimizations can be accurately obtained more quickly and efficiently during the chip design process (col. 2, ll.55-61).

Allowable Subject Matter

13.   Claims 13, 16, 24, 25 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record

does not teach comprising adjusting the threshold value to change the balance between the objective function and the cost; the cost comprises at least one of a layout cost which represents at least one layout resource required to lay out a cell corresponding to the at least one cell type, and a verification cost which represents at least one verification resource required to test a cell corresponding to the at least one cell type; the profit function relates an area gain for a given number of subtypes for the parent cell instances to a layout cost associated with the given number of subtypes; the circuit design corresponds to a hierarchy having a word level, and wherein partitioning the cells instances for each cell type into the first plurality of subtypes comprises partitioning all cell instances corresponding to the word level and any level of the hierarchy below the word level.
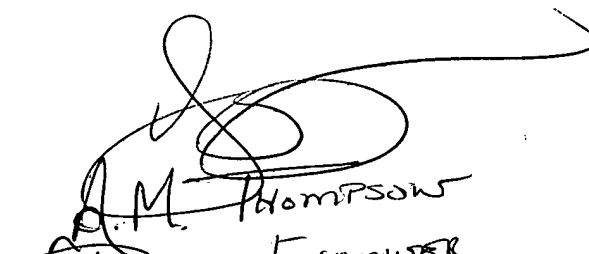
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen B Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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